OMTI 5090

Scientific Micro Systems, Inc.

OMTI 5090
IBM PC BUS INTERFACE CHIP
REFERENCE MANUAL
JUNE 1985

PUBLICATION NO. 3001238

OMTI 5090

IBM PC BUS INTERFACE CHIP

REFERENCE MANUAL

SCIENTIFIC MICRO SYSTEMS, INC.
339 North Bernardo Avenue
P.O. Box 7777
Mountain View
CALIFORNIA 94039

TEL: 415-964-5700
TWX: 910-3379-6577

DOCUMENT NUMBER: 3001238

REVISION: A

DATE OF THIS REVISION: 7 JUNE, 1985

TABLE OF CONTENTS

SECTION 1

INTRODUCTION

1.1 GENERAL

The I/O Channel Interface is a special purpose CMOS VLSI component which provides the circuitry necessary for interfacing a controller to the I/O Channel bus of the IBM Personal Computer (PC XT or PC AT). The chip provides a buffered data path to and from the I/O Channel, address decoding for access to 8 I/O ports, address decoding for access to an external BIOS ROM, and circuitry for control of bus interrupts and DMA transfers.

1.2 FUNCTIONAL ORGANIZATION

A typical system configuration showing the use of the chip is illustrated in Figure 1-1.

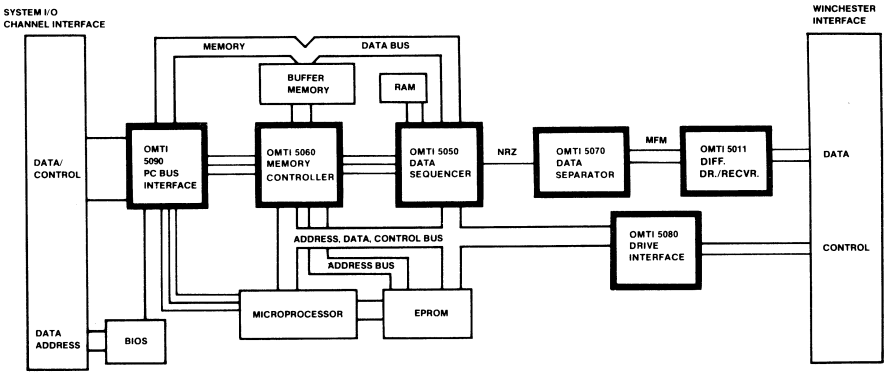
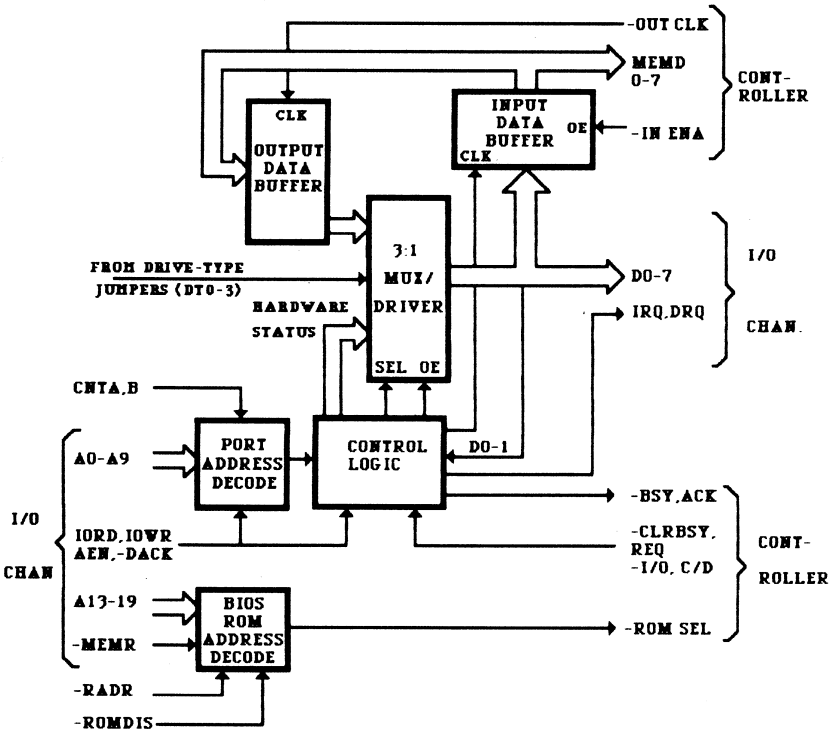


Figure 1-2 shows a block diagram of the I/O Channel Interface chip. Each of the blocks is described below.



BLOCK DIAGRAM
Figure 1-2

The Port Address Decode Block decodes address lines A0-A9 from the I/O Channel to allow selection of eight I/O ports: four write ports and four read ports (of which only three are used). Two address select input pins (-CNTA and -CNTB) are provided to change the address reange of the I/O ports so as to allow support of multiple controllers on the same PC. The four possible address ranges are as follows:

320 - 323
324 - 327
328 - 32B
32C - 32F

Paragraph 2.1 describes the I/O ports in more detail.

The BIOS Address Decode block decodes address lines A13-A19 from the I/O Channel to give a ROM select signal (-ROMSEL) for enabling reads of an external 8K BIOS ROM. An address select input pin (-RADR) is provided t6o change the address range of the ROM. The two ranges are as follows:

C8000 - C9FFF
CA000 - CBFFF

An input pin (-ROMDIS) is also provided to disable the decoding of the BIOS ROM address entirely.

The Control Logic block contains various circuitry to control I/O port register reads and writes, I/O channel DMA transfers, and I/O channel interrupts.

The 3:1 Mux/Driver block allows one of three different I/O ports to be read on the I/O channel by the PC. These ports are the Output Data Buffer (Port 0), which latches data from the controller's MEMD 0-7 bus; the Hardware Status (Port 1), which reflects the state of various control signals inside the I/O Channel Interface chip; and the Drive Type (Port 2) which allows the PC to read the value of four inputs (DT3-DT0), which specify the type of disk drive in use. (Note that a fourth I/O read port address exists, but the I/O channel data bus is not driven if Port 3 is read.) The Input Data Buffer latches data from the I/O Channel data bus D0-D7. Its output may be enables onto the controller's MEMD 0-7 data bus by asserting the signal - INENA.

SECTION 2

DESCRIPTION

2.1 I/O PORTS

The I/O Channel Interface decodes eight I/O Port addresses; four read and four write. Up to four controllers may exist in a system and they must have unique port addresses, thus the two address select inputs -CNTA and -CNTB are provided to select the port address range.

The port addresses are as follows:

PORT ADDRESSES CONTROLLER NUMBER				PORT NAME
0	1	2	3	
320	324	328	32C	PORT 0
321	325	329	32D	PORT 1
322	326	32A	32E	PORT 2
323	327	32B	32F	PORT 3

Each port has a different function depending on whether it is read or written. The functions are briefly described below.

PORT NAME	READ/WRITE	FUNCTION
Port 0	Read	Host reads Output Data Buffer
Port 0	Write	Host writes Input Data Buffer
Port 1	Read	Host reads Hardware Status
Port 1	Write	Host issues Software Reset
Port 2	Read	Host reads DT0-DT3 pins
Port 2	Write	Host issues Select signal
Port 3	Read	(Not Used)
Port 3	Write	Host sets DMA/Interrupt Enable Bits

A more detailed description of the ports is given in the following paragraphs.

PORT 0 READ

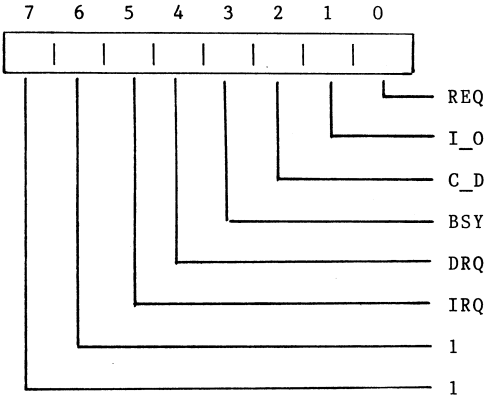
This port is read by the fost; either explicitly via a programmed I/O instruction, or implicity during a DMA transfer to the host. The data is read from the Output Data Buffer, and is assumed to have been previously latched into there from the MEMD 0-7 bus by the signal -OUTCLK.

PORT 0 - WRITE

This port is written to by the host; either explicitly via a programmed I/O instruction, or implicitly during a DMA transfer from the host. The write data is latched into the Input Data Buffer, and is assumed to be subsequently read from there onto the MEMD 0-7 bus by the signal -INENA.

PORT 1 - READ

This port is read by the host to determine the hardware status of the I/O Channel Interface. The bits are defined as follows:



Bit 0 reflects the state of the REQ input pin. When set, it indicates that the controller expects a byte of data to be either written to, or read from, Port 0. This includes the special case of Port 0 usage during a DMA transfer.

Bit 1 reflects the opposite state of the -I_O input pin. When set, it indicates that the direction of data transfer through port 0 is IN to the host (i.e. a port 0 read or a DMA write-to-memory). When reset, it indicates that the data is OUT of the host (i.e. a port 0 write or a DMA read-from-memory).

Bit 2 reflects the state of the C_D input pin. When set, it indicates that data transfers through port 0 contain Control information. When reset, it indicates that data transfers through

port 0 are of a different nature (usually read/write data from/to a disk drive).

The I/O Channel Interface hardware is designed to generate an interrupt (if enabled) when REQ is asserted if C_D is high and -I_O is low. The I/O Channel Interface hardware is designed to generate a DMA request (if enabled) when REQ is asserted if C_D is low.

Bit 3 reflects the inverse of the -BSY output signal. It represents the output of a flip-flop which is set by writing to port 2 (the select operation), and is cleared by the input signal -CLRBSY.

Bit 4 is set when the I/O Channel interface is asserting the DRQ output signal.

Bit 5 is set when the I/O Channel interface is asserting the DRQ output signal.

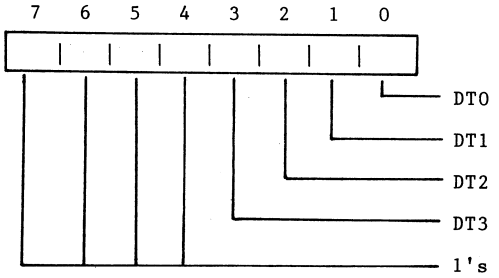
Bits 6 and 7 always read as 1's.

PORT 1 - WRITE

The host writes to this port to generate a software reset. This action will produce a pulse on the outputs -RSTSOFT and -RSTOUT, will clear the DMA/Interrupt Enable bits, and will clear the BSY flip-flop. The width of the pulse on -RSTSOFT and -RSTOUT is dependent on the external network connectged to the pin -RSTCAP.

PORT 2 - READ

This port is read by the host to determine the stater of the DTO-3 input pins. The bits are defined as follows:



Bits 0 to 3 reflect the state of input pins DTO to DT3.

Bits 4 to 7 always read as 1's.

PORT 2 - WRITE

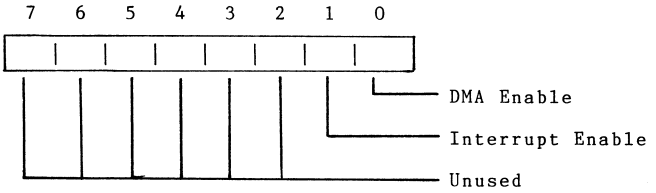
The host writes to this port to "select" the controller. This action causes the BSY flip-flop to set, and the -BSY output signal to be asserted.

PORT 3 - READ

This port is not used, and if read will not assert data on the D7-D0 bus.

PORT 3 - WRITE

The host writes to this port to set the DMA/Interrupt Enable bits. The bits are defined as follows:



When bit 0 is set, the DRQ output signal will be asserted when the REQ input goes high if the C_D input is low.

When bit 1 is set, the IRQ output signal will be asserted when the REQ input goes high if the C_D input is high and the -I_O input is low.

Bits 2 through 7 are unused.

SECTION 3

INTERFACING

3.1 PIN DESCRIPTIONS

SYMBOL	TYPE	NAME AND FUNCTION
A9-A0 A19-A13	I	ADDRESS BUS System I/O channel address bus (active high). A9-A0 contain I/O port addresses; A19-A0 contain memory mapped addresses for access to external ROM (see -ROMSEL).
D7-D0	I/O	DATA BUS System I/O channel data bus (active high). These bi-directional, tri-state lines are used to transfer data, commands and status.
-IORD	I	I/O READ System I/O channel signal which is asserted to read data from an I/O port address (AEN is not active and port address is on A9-A0), or to read data from a device during a DMA cycle (AEN is active and the device is selected by the -DACK signal being active).
-IOWR	I	I/O WRITE System I/O channel signal which is asserted to write data to an I/O port address (AEN is not active and port address is on A9-A0), or to write data to a device during a DMA cycle (AEN is active and the device is selected by -DACK being active).
AEN	I	ADDRESS ENABLE System I/O channel signal which is asserted during a DMA cycle. It is used to disable the decoding of I/O port addresses during DMA cycles.
RSTIN	I	RESET DRIVER IN /system I/O channel signal which is asserted when the system power supplies are outside their specified range of outputs. Used during power-up to initialize device logic.
IRQ	O	INTERRUPT REQUEST System I/O channel signal which is asserted by the device to cause an interrupt request. The output is tri-stated when interrupts are disabled.

DRQ	O	DMA REQUEST System I/O channel signal which is asserted by the device to cause an DMA request. The output is tri-stated when interrupts are disabled.
-DACK	I	DMA ACKNOWLEDGE System I/O channel signal which is asserted to indicate that a DRQ signal has been honored. -DACK will clear the DRQ signal, and in conjunction with iether -IORD or -IOWR, will cause DMA data to read from, or written to the device.
-MEMR	I	MEMORY READ System I/O channel signal which is asserted during memory read cycle, indicating that the memory (in this case the external ROM) should put its data on D7-DO.
MEMD7-MEMDO	I	MEMORY DATA Internal bi-directional data bus. This is the path by which data is transferred to and from the controller buffer.
-RSTOUT	O	RESET OUT This signal is the NOR of: a) RSTIN b) the programmed reset signal generated by writing to PORT 1 (lengthened by a monostable) c) an internal power-on-reset circuit.
-BSY	O	This signal is the output of a flip-flop which is set when the host system writes to PORT 2, and is cleared by the -CLRBSY signal.
REQ	I	REQUEST This signal indicates a request for transfer of data on the system I/O channel.
ACK	I	ACKNOWLEDGE This signal is the output of a flip-flop which is set when a system I/O channel transfer has been completed. The signal is generated in response to the REQ signal and is cleared when REQ is inactive.

-I_O I

INPUT/OUTPUT
This signal indicates the direction of data transfer across the system I/O channel. A low level on this pin means transfer INto the host; a high level on this pin means transfer OUT of the host (i.e. into the device).

C_D I

CONTROL/DATA
This signal indicates the tpe of data transfer that is in progress across the system I/O channel (REQ is asserted). A high level on this pin indicates that control information is being transferred (command bytes or completion status byte). A low level on this pin indicates that other data (DMA, request-sense etc.) is being transferred.

-CLRBSY I

CLEAR BUSY
This input is used to clear the BSY flip-flop on its leading (falling) edge.

-INENA I

INPUT DATA BUFFER ENABLE
This input enables the data latched in the Input Data Buffer from the system I/O channel, onto the MEMD7-MEMD0 bus.

-OUTCLK I

OUTPUT DATA BUFFER CLOCK
This input latches data on its trailing (rising) edge from the MEMD7-MEMD0 bus into the Output Data Buffer prior to its being transferred on the system I/O channel.

DT3-DT0 I

DRIVE TYPE
These internally pulled-up lines allow input of a drive-type (or other) code which can be read from Port 2 by the host system.

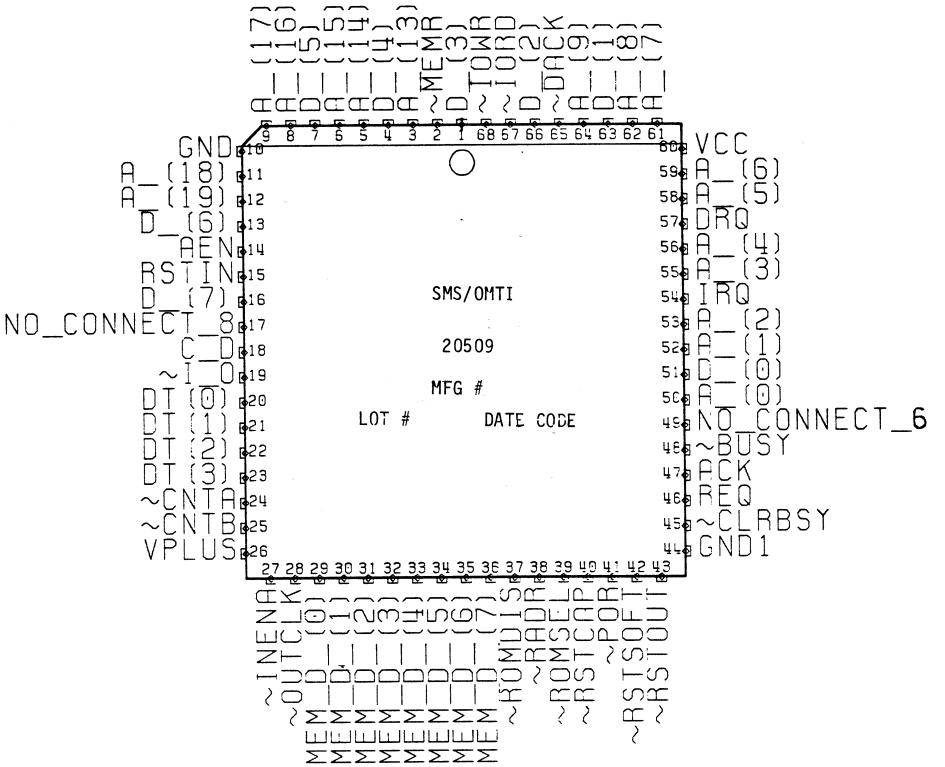
-CNTA I
-CNTB

CONTROLLER ADDRESS
These inputs (internally pulled-up) allow selection of controller port address as follows:

CNTB	CNTA	PORT ADDRESS RANGE (A9-A0)
H	H	320 - 323
H	L	324 - 327
L	H	328 - 32B
L	L	32C - 32F

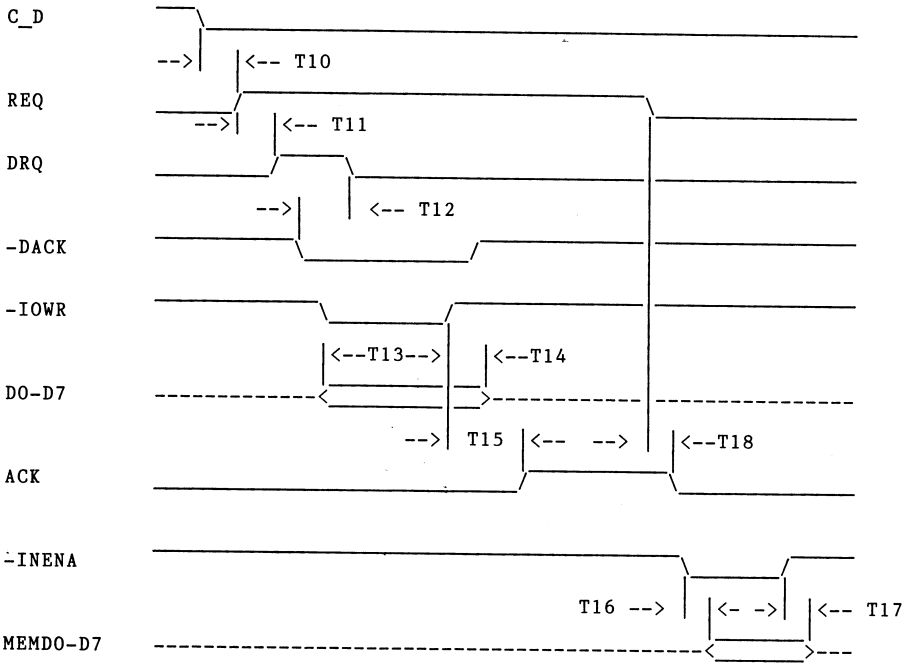
-ROMSEL	O	ROM SELECT When the signal -RADR is high, this output is asserted when A19-A13 contain the binary value 1100100, the signal -MEMR is low, and the signal -ROMDIS is high. When the signal -RADR is low, this output is asserted when A19-A13 contain the binary value 1100101, the s8ignal -MEMR is low, and the signal -ROMDIS is high. This signal is used to enable an external ROM onto the data bus D7-D0.
-RADR	I	ROM ADDRESS This internally pulled-up input controls the address decoding for the signal -ROMSEL (see above).
-RSTCAP	I/O	RESET CAPACITOR This line is used to connect an external timing capacitor to control the pulse width of a monostable which is fired by a programmed reset from the host.
-POR	O	POWER ON RESET This signal is an inverted version of the input signal RSTIN.
-RSTSOFT	O	SOFTWARE RESET This signal is an active low output generated by writing to Port 1 (lengthened by a monostable), or by an internal power-on-reset circuit.
-ROMDIS	I	ROM DISABLE When this internally pulled-up signal is low, the address decoding of the signal -ROMSEL is disabled.

3.2 PIN ASSIGNMENT

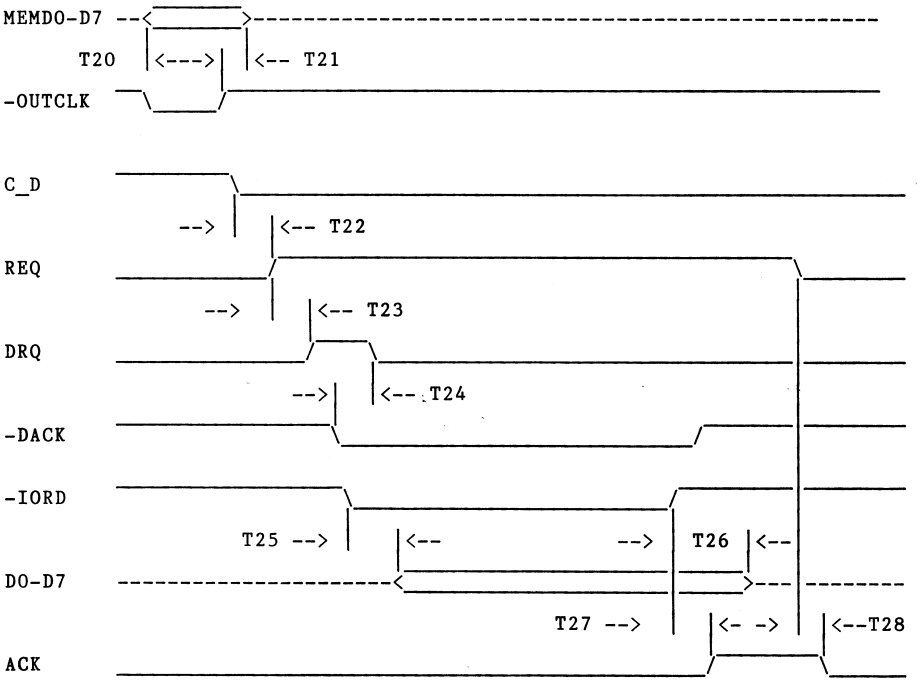


3.3 TIMING REQUIREMENTS

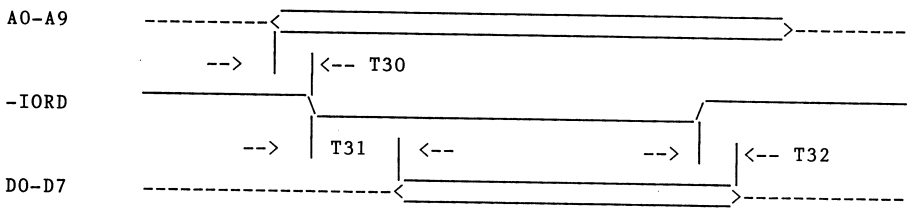
3.3.1 DMA READ Cycle (Host to Buffer)



3.3.2 DMA WRITE Cycle (Buffer to Host)

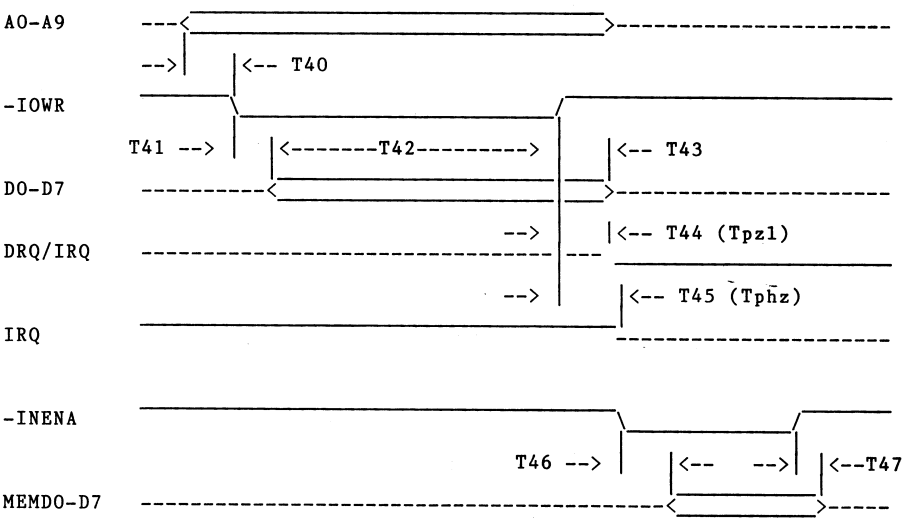


3.3.3 I/O PORT READ Cycle

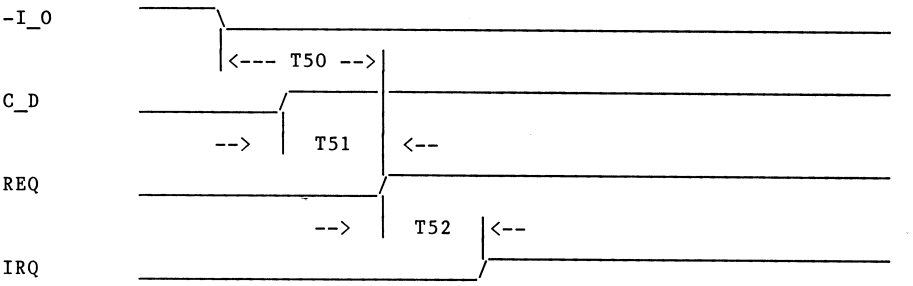


3.3.4 I/O PORT WRITE Cycles

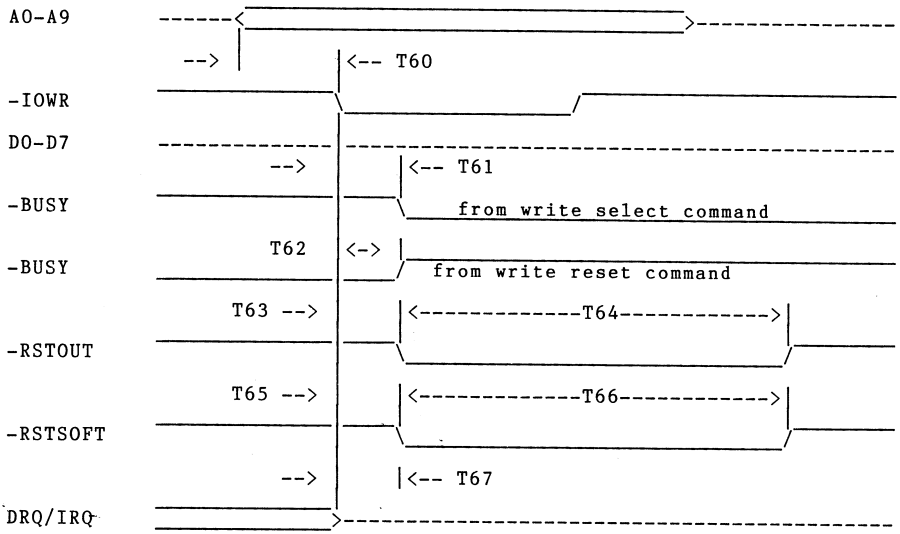
3.3.4.1 WRITE DATA,DRQ/IRQ Mask Bit Cycle



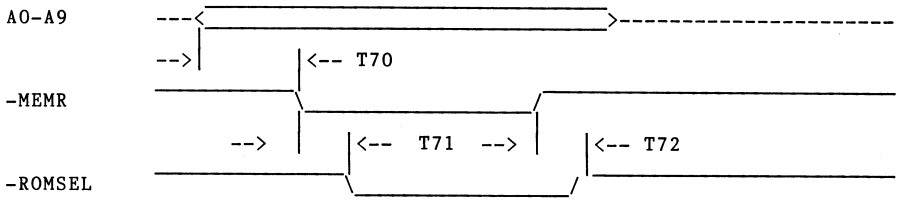
3.3.4.2 IRQ SETUP TIMES



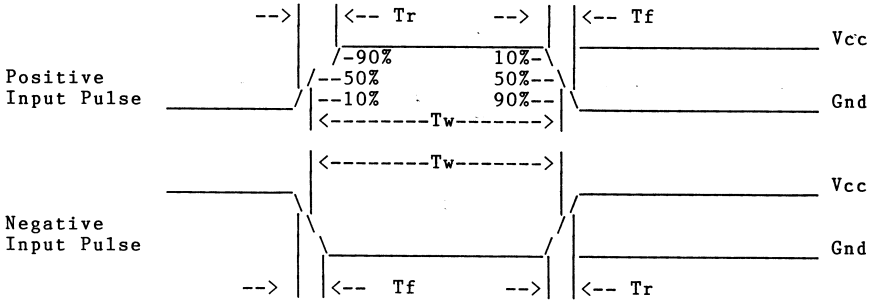
3.3.4.3 WRITE SELECT/RESET CYCLE



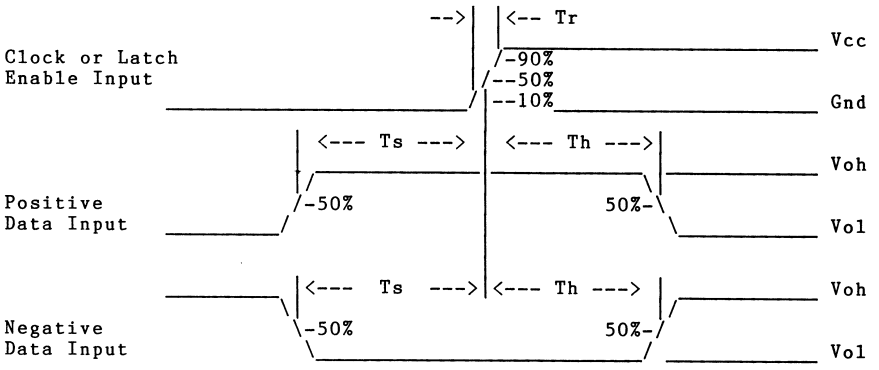
3.3.5 BIOS ROM READ



3.3.6 INPUT PULSE WIDTH WAVEFORMS



3.3.7 SETUP AND HOLD TIME WAVEFORM DEFINITIONS



3.3 TIMING REQUIREMENTS continued

Symbol	Figure	Parameter	Min	Max	Unit
		DMA READ (HOST TO BUFFER)			
T10	3.3.1	SETUP TIME FROM C/D TO REQ	25		nsec
T11	3.3.1	DELAY FROM REQ TO DRQ HI		35	
T12	3.3.1	DELAY FROM DACK TO DRQ LO		35	
T13	3.3.1	DATA SETUP TIME	25/90*		
T14	3.3.1	DATA HOLD TIME	25/30*		
T15	3.3.1	DELAY FROM IOWR TO ACK HI		35	
T16	3.3.1	DELAY TO DATA VALID		35	
T17	3.3.1	DELAY TO DATA INVALID		35	
T18	3.3.1	DELAY FROM REQ TO ACK LO		35	
		DMA WRITE (BUFFER TO HOST)			
T20	3.3.2	DATA SETUP TIME	25		nsec
T21	3.3.2	DATA HOLD TIME	20		
T22	3.3.2	SETUP TIME FROM C/D TO REQ	25		
T23	3.3.2	DELAY FROM REQ TO DRQ HI		35	
T24	3.3.2	DELAY FROM DACK TO DRQ LO		35	
T25	3.3.2	DELAY TO DATA VALID		35/240*	
T26	3.3.2	DATA HOLD TIME	4*/25	35/60*	
T27	3.3.2	DELAY FROM IORD TO ACK HI		35	
T28	3.3.2	DELAY FROM REQ TO ACK LO		35	
		I/O PORT READ			
T30	3.3.3.1	ADDRESS SETUP TIME	25/90*		nsec
T31	3.3.3.1	DELAY TO DATA VALID		35/550*	
T32	3.3.3.1	DATA HOLD TIME	10*/25	35/60*	
		I/O PORT WRITE			
T40	3.3.4.1	ADDRESS SETUP TIME	30/90*		nsec
T41	3.3.4.1	DELAY TO DATA VALID		35/110*	
T42	3.3.4.1	DATA SETUP TIME	25/515*		
T43	3.3.4.1	DATA HOLD TIME	25/95*		
T44	3.3.4.1	DELAY FROM IOWR TO IRQ/DRQ		45	
T45	3.3.4.1	DELAY FROM IRQ HI TO TRISTATE		45	
T46	3.3.4.1	DELAY TO DATA VALID		35	
T47	3.3.4.1	DELAY TO DATA INVALID		35	
		IRQ SETUP TIMES			
T50	3.3.4.2	I_O SETUP TIME	25		nsec
T51	3.3.4.2	C_D SETUP TIME	20		
T52	3.3.4.2	DELAY FROM IRQ LO TO HI		35	

Symbol	Figure	Parameter	Min	Max	Unit
		WRITE SELECT/RESET			
T60	3.3.4.3	ADDRESS SETUP TIME	30/90*		nsec
T61	3.3.4.3	DELAY FROM IOWR TO BUSY		35	nsec
T62	3.3.4.3	DELAY FROM IOWR TO BUSY		35	nsec
T63	3.3.4.3	DELAY FROM IOWR TO RSTOUT		45	nsec
T64	3.3.4.3	#PULSE WIDTH		2	nsec
T65	3.3.4.3	DELAY FROM IOWR TO RSTSOFT		45	nsec
T66	3.3.4.3	#PULSE WIDTH		2	nsec
T67	3.3.4.3	DELAY TO DRQ/IRQ HI IMPEDANCE		60	nsec
		#Dependent on external capacitor			
		BIOS ROM READ			
T70	3.3.5	ADDRESS SETUP TIME	20		nsec
T71	3.3.5	DELAY FROM MEMR TO ROMSEL LO		20	
T72	3.3.5	DELAY FROM MEMR TO ROMSEL HI		20	
Tw	3.3.6	*PULSE WIDTH	35		nsec
Tr	3.3.6	*RISE TIME		10	
Tf	3.3.6	*FALL TIME		10	
		*Generic requirements			

Note: When the double entry format t1/t2* is used, the following conditions apply:

a) The value identified with an "*" (in this case t2) is derived from an IBM specification and may contain some degree of error.

b) The other value listed (t1) is what was actually used as a maximum or minimum design limit.

Typical Conditions	Maximum Conditions
Vcc = 5.00 Volts	Vcc = 4.75 Volts
Ta = 25 degrees C	Ta = 70 degrees C
Cl = 50 pF (single drivers)	Cl = 50 pF
Cl = 150 pF (double drivers)	Cl = 150 pF

SECTION 4

ELECTRICAL CHARACTERISTICS

4.1 DC CHARACTERISTICS

TYPICAL OPERATING CONDITIONS

Parameter	Min	Max	Unit
Supply Voltage (Vcc)	+4.75	+5.25	Volts
DC Input/Output Voltage (Vin,Vout)	0.0	Vcc	Volts
Ambient Operating Temperature(Ta)	0	+70	degrees C
Input Rise/Fall Times (Tr,Tf)		6	nsec
DC Output per Pin: (Vol = 0.5 Volts)			
Single Driver		6.0	mA
Double Driver		12.0	mA
Power Disipation: (Write Cycle @ 5Mhz)		35	mW

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
Supply Voltage (Vcc)	0.5	+7.00	Volts
DC Input Voltage (Vin)	0.5	Vcc+0.5	Volts
DC Output Voltage (Vout)	0.5	Vcc+0.5	Volts
Input Rise/Fall Times (Tr,Tf)		500	nsec
Clamp Diode Current (Iik, Iok)		+5.0	mA
DC Output per Pin: (Vol = 0.5 Volts)			
Single Driver		9.0	mA
Double Driver		18.0	mA
Power Disipation: 70 degreesC, Vcc max.		100	mW
Storage Temperature	65	+150	degrees C

Parameter		Condition	Min.	Max.	Unit
Voh	High Level Output Voltage, Single Driver	Vcc = Min Ioh = 4.0mA	2.4		Volt
Voh	High Level Output Voltage, Double Driver	Vcc = Min Ioh = 8.0mA	2.4		Volt
Vol	Low Level Output Voltage, Single Driver	Vcc = Min Iol = 6.0mA		0.5	Volt
Vol	Low Level Output Voltage, Double Driver	Vcc = Min Iol = 12.0 mA		0.5	Volt
Vih	High Level Input Voltage	Bus Interface pins All others	2.0 2.4		Volt Volt
Vil	Low Level Input			0.8	Volt
*Iih	High Level Input Current	Vcc = Max Vin = 2.7Volt		+10.0	uA
*Iil	Low Level Input Current	Vcc = Max Vin = 0.4 Volt		+10.0	uA
Iozh	OffState Output Current, High Level Voltage Applied	Vcc = Max Vout = 2.7 Volt		+10.0	uA
Iozl	OffState Output Current, Low Level Voltage Applied	Vcc = Max Vout = 0.4 Volt		+10.0	uA
Icc	Quiescent Supply Current, Input pins with internal pull ups not connected	Vcc = Max Ta = Max		TBD	uA

* Does not include pins with internal active pullups.

SECTION 5

SPECIFICATIONS

5.1 MECHANICAL SPECIFICATIONS